

IN THE SPECIFICATION:

At page 5, first paragraph under the heading "Summary of the Invention," replace that paragraph with the following paragraph:

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A1
There exists a need to develop a semiconductor integrated circuit capacitor that does not suffer from the aforementioned infirmities. Accordingly, the present invention is directed to a semiconductor integrated circuit capacitor and its fabricating method that substantially obviates one or more of the problems due to the limitations and the disadvantages of the related art. A feature of the present invention therefore is to provide a semiconductor integrated circuit capacitor, and a method of effectively making the capacitor. The inventive capacitor preferably is used in a logic circuit and/or an analog circuit.

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The changes in the previous paragraph are indicated by brackets for deletions and underlining for insertions.

There exists a need to develop a semiconductor integrated circuit capacitor that does not suffer from the aforementioned [infirmaries] infirmities. Accordingly, the present invention is directed to a semiconductor integrated circuit capacitor and its fabricating method that substantially obviates one or more of the problems due to the limitations and the disadvantages of the related art. A feature of the present invention therefore is to provide a semiconductor integrated circuit capacitor, and a method of effectively making the capacitor. The inventive capacitor preferably is used in a logic circuit and/or an analog circuit.

At page 9, third new paragraph, replace that paragraph with the following paragraph:

A2 In the inventive process, the layer patterning characteristic can be enhanced, and the contact resistance between the insulating layer 200 and the lower electrode 202a can be decreased by forming the first wire line 202b and the lower electrode 202a in a particularly preferred manner. In this embodiment, the first wire line 202b and the lower electrode 202a are formed and etched by using a photoresist pattern (not shown) as a mask to define both a capacitor formation part and a wire line formation part. The first wire line 202b and the lower electrode 202a preferably are formed by successively depositing a metal barrier layer (not shown), the first conductive layer and an anti-reflection layer (not shown) on the insulating substrate 200. The metal barrier layer and/or the anti-reflection layer can be: (i) a single-level structure containing a material selected from Ti, Ta, Mo, TiN, TiW, TaN, and MoN; and/or (ii) a multi-level structure containing materials selected from W-N, W-Si-N, Ta-Si-N, W-B-N, and Ti-Si-N; and/or (iii) combination layers of (i) and (ii).

The changes in the previous paragraph are indicated by brackets for deletions and underlining for insertions.

In the inventive process, the layer patterning characteristic can be enhanced, and the contact resistance between the insulating layer 200 and the lower electrode 202a can be decreased by forming the first wire line 202b and the lower electrode 202a in a particularly preferred manner. In this embodiment, the first wire line 202b and the lower electrode 202a are formed and etched by using a photoresist pattern (not shown) as a mask to define both a capacitor formation part and a wire line formation part. The first wire line 202b and the lower electrode 202a preferably are formed by successively depositing a metal barrier layer (not shown), the first conductive layer and an anti-reflection layer (not shown) on the insulating substrate 200. The metal barrier layer and/or the anti-reflection layer can be: (i) a single-level structure containing a material selected from Ti, Ta, Mo, TiN, TiW, TaN, and MoN; and/or (ii) a multi-level structure containing materials selected from W-N, W-Si-N, Ta-Si-N, W-B-N, and Ti-Si-N; and/or (iii) [mixtures] combination layers of (i) and (ii).